Considerations for
Bulk CMOS to FD-SOI Design Porting

Release 0.1.a
September, 2011

ABSTRACT
The scope of this study is to examine the efforts required for a straight “port” of an existing bulk CMOS design to FD-SOI at the same node. The objective would be to get value from FD-SOI for a modest redesign effort – even if this means not necessarily taking maximum advantage of the potentialities of FD-SOI. The focus is on FD-SOI with Ultra-Thin Buried Oxide. This document intends to be sufficiently generic to be applicable to different possible implementations of the FD-SOI technology by foundries.

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INTRODUCTION

The scope of this study is to examine the efforts required to port existing bulk CMOS designs to FD-SOI at the same node. The objective of such a straight "porting" would be to get value from FD-SOI for a modest redesign effort, even if this means not taking full advantage of the potentialities of FD-SOI. Different perspectives may be taken:

- IP Porting: The focus may be to make sure that all IPs available in Bulk can easily be ported to FD-SOI, accepting some redesign work at System-on-Chip (SOC) integration level.
- Full chip design porting: Alternatively, it may be important to assess the efforts needed to start from an existing SoC design on Bulk and port this full chip to FD-SOI.

This document will attempt to address both cases.

The technology considered here is Fully-Depleted SOI on Ultra-Thin Buried Oxide (less than 30nm thick), also known as UTBB, Ultra-Thin Body and BOx. It is also assumed that a bulk CMOS offering and an FD-SOI offering co-exist at the node considered (for example the 20nm technology node). Only few assumptions beyond that are made, for this document to remain sufficiently generic to be applicable to different possible implementations of the FD-SOI technology by foundries. In other words, guidelines are provided and the reality will depend on the actual foundry offering and associated PDK (Process Design Kit).

1. Porting Designs to FD-SOI (same node) – High Level Summary

Below is an estimate of the magnitude of efforts required to port designs from bulk CMOS to FD-SOI. The justifications for the ratings proposed are provided further down this document.

The key messages are:

- Designing for FD-SOI is same as designing for planar bulk CMOS.
- IP Porting from Bulk to FD-SOI (same node, same foundry) can be very direct, for worthwhile benefits at fast time-to-market – with some more work for Analog IP. Further optimization efforts can bring even greater product differentiation.
- SOC Porting from Bulk to FD-SOI can be very direct depending on FD-SOI technology offered by Foundry, especially VT offering vs. Bulk.
- FD-SOI offers efficient knobs to further optimize SOC performance In particular, (optional) back-biasing is a very powerful tool in FD-SOI to boost performance, cut leakage or further reduce corner variations.

When considering porting designs, two areas of work can be considered:
- at ‘foundation IP’ level,
- at SOC implementation level

IP Porting Efforts:

<table>
<thead>
<tr>
<th>Type of Foundation IP</th>
<th>Expected Redesign Effort</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Cell Libraries</td>
<td>Very Limited (*)</td>
</tr>
<tr>
<td>Memory Compilers</td>
<td>Very Limited (**), (*)</td>
</tr>
<tr>
<td>I/Os</td>
<td>Limited (*)</td>
</tr>
<tr>
<td>Analog and Mixed Signal</td>
<td>Limited to More Significant</td>
</tr>
</tbody>
</table>

(*) : Assuming the "worthwhile benefits at fastest time-to-market" approach is favored
(**) : Assuming availability of suitable 'native VT' – see 4.2
SoC Porting:

When considering the port of a full existing SOC (as opposed to porting the physical IPs but designing a new SOC using them), some additional considerations come into play, namely physical implementation (i.e. floorplan, cell placement, routing, etc.) and sign-off (timing checks, design rule checks, etc).

Two paths are possible:
- Path 1: straightest possible porting from Bulk to FD-SOI – as close as possible to keeping the same GDS with all FDSOI-specific updates automatically handled at mask generation,
- Path 2: FD-SOI re-optimized SOC implementation.

One important factor in determining the amount of efforts required at SOC integration level is the need or not to add a back-biasing scheme to a SOC that did not use body bias. This largely depends on the foundry’s technology implementation strategy – especially, is it offering native VTs (i.e. without specific back-bias) that match those used in the original SOC on bulk silicon CMOS? (refer to Section 3-7 and Appendix A). The table below outlines expected level of efforts and discriminates the case where back-bias is required and the case where it is not.

<table>
<thead>
<tr>
<th><strong>SOC Design Aspect</strong></th>
<th><strong>Expected Effort – for a direct SOC porting</strong></th>
</tr>
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<tbody>
<tr>
<td></td>
<td>If no introduction of Back-Bias is required</td>
</tr>
<tr>
<td>Physical Implementation</td>
<td>Limited Effort</td>
</tr>
<tr>
<td>Sign-Off</td>
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</tr>
</tbody>
</table>

2. Brief Reminder of FD-SOI Technology and Circuit-Level Benefits

Planar Fully Depleted Silicon on Insulator (FD-SOI) technology relies on an ultra-thin layer of silicon over a Buried Oxide, BOx ([Fig. 1 - Bulk and SOI Transistor Flavors]) – refer to [Faynot2011] for a technical overview or [Cauchy2010] for a simpler primer. CMOS transistors built into this top silicon layer are “ultra-thin body” devices and operate in fully-depleted mode, because the electrical channel that forms between source and drain is confined within the thin space between the gate oxide and the BOx; it is therefore more ideally controlled by the gate than in classical planar bulk CMOS. In addition, with FD-SOI technology there is no need to dope the channel – thereby mostly eliminating random dopant fluctuation which is a major source of the variability that plagues bulk CMOS at advanced nodes. As a result, FD-SOI transistors bring to designers some unique advantages outlined below.

This study focuses on the technology flavor where the buried oxide (BOx) is ultra-thin too, in the 10-30nm range. Usage of an ultra-thin BOx, on top of device-related benefits (relaxing silicon thinness requirements and better transistor characteristics for some parameters), brings:

- the ability to apply back-biasing, which is a technique usable for tuning the performance/leakage trade-off, discussed further down this document and in Appendix A.
- the ability during the fabrication process to implant heavily doped “back-planes” or “ground-planes” under the BOx, for VT adjustment (as outlined in Appendix B) and/or for best efficiency of the back-bias.
- the option during the fabrication process to locally remove top silicon and BOx to reach the base silicon and co-integrate devices on SOI and (non geometry-critical) devices on Bulk, with a small step height between an SOI zone and a Bulk zone, compatible with lithography tools – refer to Fig. 2 – Co-integration of Bulk and FD-SOI Devices.
The key benefits of FD-SOI vs. planar bulk CMOS at circuit level include:
- At equivalent leakage, clear performance boost through faster operation, with the relative performance gap growing tremendously in the low Vdd range (specifically, as Vdd gets closer to VT),
- Or, conversely, ability to reach the same operating frequency specification at significantly lower Vdd, enabling large power savings,
- Drastically reduced variability, with a positive impact on VDDmin of SRAM arrays, chip-level leakage, etc.
- Ability to operate full designs at very low Vdd (e.g. down to 0.5-0.6V) – consequence of the former benefits,
- Excellent responsiveness to back-bias,
- Enhanced efficiency of other low-power design techniques such as DVFS (Dynamic Voltage and Frequency Scaling), power switches, etc. by virtue of the above characteristics.

The design techniques classically used in bulk CMOS are compatible with FD-SOI. One particular case is body-bias (i.e. shifting well bias voltage away from Gnd/Vdd), which must be transposed as back-bias on FD-SOI: the principle is essentially the same, with bias voltage now applied under the BOx of the target transistors.

3. FD-SOI Specificities vs. Bulk to take into account for design porting

The design flows and design methodologies to design on FD-SOI are the same as those classically used with bulk CMOS, building upon SPICE models suitable for FD-SOI devices. It
may be worth also noting that FD-SOI does not exhibit the floating body effects or kink effects associated to Partially-Depleted SOI.

The FD-SOI specificities are more at technology level than at design level. However, especially in the context of a porting from Bulk to FD-SOI at the same node, some technological aspects can be relevant to certain designs; they are listed below.

Some of these factors are intrinsic to the nature of the FD-SOI technology, others depend on what the exact FD-SOI offer of the selected foundry would be – in particular what choices the foundry would make in terms of device menu, device implementation strategy etc. Their impact on the different design domains will be addressed in the next section.

**Devices and Technology Intrinsic:**

- “Non-thin film friendly” devices esp. ESD diodes
- Different Electrical Characteristics
  - a) Logic Timings
  - b) Analog behavior
  - c) Nmos/Pmos current ratio
  - d) Possible self-heating in specific conditions
- Antenna Protections
- Parasitic Bipolar – if applicable
- Better Variability & Matching, Lower Sensitivity to PVT corners

**Technology Implementation Dependent:**

- Additional Design Rules – if any
- VT menu
- Back-Bias (if used)

**Some details:**

### 3.1 Non-thin film friendly devices e.g. ESD diodes:

There are a few devices that rely on the existence of a sufficiently large volume of silicon to fulfill their role, which may be problematic on ultra-thin SOI – for example devices that must withstand large surges of current, like ESD protection diodes.

The foundry may decide to keep these devices on Bulk, through hybrid Bulk-FDSOI co-integration (e.g. by locally etching off the top silicon and the BOX). Or, it may replicate them on SOI (possibly involving some local silicon growth to increase its thickness), and it is up to the user to instantiate them with adequate sizes to fit his needs. In such cases the impact on design is minimum, as the designer does not really care how the device is fabricated and just wants to use it properly.

In some rare instances, the foundry could decide not to provide a particular device and provide an alternative instead (for example no substrate diodes, use lateral diodes instead) – then the design must be tuned to cope with this.

**Possible Impact on:** porting of I/Os, of Analog IP, of some specialty physical IP

### 3.2 Different Electrical Characteristics:

- a) Logic Timings

At equivalent Ioff, FD-SOI logic paths should normally be faster than their planar Bulk counterparts.

**Impact on:** characterization of Standard Cells, Memory Compilers, I/Os – SoC Sign-Off
b) **Analog Behavior**
Differences in I-V curves, capacitance etc. of FD-SOI transistors will also impact key analog characteristics such as intrinsic gain, Early voltage, frequency noise etc.

*Possible Impact on: porting of Analog and Mixed Signal IP Designs*


c) **Different Electrical Characteristics : Nmos/Pmos current ratio**
The ratio of NFET and PFET drive current per unit width (mA/um) may be somewhat different for the FD-SOI technology and the Bulk technology considered. This may, to some extent, lead to different optimal sizing of nmos and pmos transistors in CMOS structures. The penalty for not fine-tuning n/p ratios is, however, expected to be relatively small, and probably acceptable in many cases (however, obviously, this will have to be confirmed with the characteristics of the technology actually offered by the foundry).

*Possible Impact: optimization of standard cells and memories – if best-optimized performance is sought*

d) **Self-heating (only in some specific conditions)**
Self-heating is relevant only to the design of circuits that involve fairly large DC or quasi-DC currents [Jin2001]. If a significant current flows continuously then the temperature within the device in which this current flows may rise locally and cause a local reduction of drive current. Experience shows that self-heating does not jeopardize intended functionality of circuits. Using an ultra-thin BOX should also alleviate this [Ishigaki2010]. For most accurate SPICE simulation of circuits that involve quasi-DC currents, however, it may be preferable to run simulations with a self-heating switch turned ‘on’.

*Possible Impact on: simulation of some Analog IP or some I/Os*

### 3.3 Antenna Protections

The presence of the BOX that isolates the substrate from the active silicon needs to be taken into account, as some antenna protections rely on the ability to evacuate through the substrate charges that would build up on long metal wires during the fabrication process.

*Possible Impact: Antenna Discharge Cells, Memory Compilers, AMS IPs, SOC Integration*

### 3.4 Parasitic Bipolar Transistor – if applicable

At high drain voltages, some FD-SOI transistors might exhibit a parasitic bipolar behavior. Again, this is more a concern for technologists than designers, who should nevertheless be warned by the foundry if this may happen, and if so, for which devices and under which conditions (esp. at what minimum drain voltage) to then take appropriate measures such as e.g. transistor stacking. Note however that this is becoming a vanishing concern for modern technologies for which VDD always stays at relatively low values. No concerns over risks of triggering a parasitic bipolar at practical drain voltages have been reported so far in publications dealing with FD-SOI technology at advanced nodes.

*Possible Impact: porting of IOs and Analog&Mixed Signal IP (only if technology exhibits this effect)*

### 3.5 Better Variability & Matching, Lower Sensitivity to PVT corners

FD-SOI exhibits much better random variability than planar bulk CMOS, and is also expected to bring lower change of characteristics from nominal PVT conditions to corner PVT conditions. This can help in the remapping of some designs.

*Possible Impact: Facilitation of porting of Analog & Mixed Signal IP and of SOC sign-off.*

### 3.6 Additional Design Rules. – if any :

It cannot be excluded that the FD-SOI process introduces a few new design rules, even though they are not expected to bring major restrictions vs. design rules used for the original Bulk design.

One typical example could be, in cases where the foundry offers Bulk and FD-SOI co-integration on the same chip, new rules at the boundary between an SOI zone and a bulk zone – like e.g. a minimum distance between an active area on SOI and an active area on bulk, etc.

*Possible Impact: Implementation/Verification of IPs and SOC*
3.7 VT Menu

The foundry will decide what VT menu to offer and how native VT values will be aligned with those offered in bulk CMOS technology at the same node.

One interesting option is to have a set of VT flavors with $I_{off}$ similar to those of the bulk CMOS technology, or at least to those used by the type of designs that are primary targets of the FD-SOI technology (which are, typically, advanced low-power Mobile and Consumer Multimedia SOCs), as illustrated in Fig. 3 – Good fit between bulk VT used by original SoC and foundry’s VT menu in FD-SOI. This option will favor porting at minimum effort, as explained further down this document.

Some deviations from this situation may be manageable without much concern. For example, $I_{off}$ does not necessarily need to be exactly matched for all transistor flavors, or it may be acceptable to live with less VT flavors in the FD-SOI version – as long as swapping bulk transistors or bitcells for their FD-SOI counterpart having closest available $I_{off}$ brings a worthwhile performance boost for comparable or better leakage power at circuit level.

An alternative option for the foundry may be to provide a set of native VT values that need to be shifted to the application’s target by block-level static back-bias (see Appendix A). This is, however, more intrusive at design porting level, as explained further down this document.

**Possible Impact:** SRAM compilers - SOC Physical Implementation – SOC Sign-Off

3.8 Back-Bias

*Note for the interested reader, Appendix A investigates further the fundamentals and implications of back-bias.*

With FD-SOI on ultra-thin BOX, the substrate underneath the BOX is normally tied to Vdd or Gnd, thus avoiding any disturbance into the channel due to a “floating back-gate” effect. In that case, there is no
intention to use back-bias to shift the VT or Ion/Ioff operating point. This is not disruptive for the design and is handled by substrate ties exactly in the same way as well biasing in handled in classical bulk CMOS technology, see next chapter (“Substrate Tie Cells” in Section 4.1).

Then there is the option to have what we will call “active” back-bias in this document, to shift the VT or, equivalently, the Ion/Ioff operating point – by shifting the voltage applied under the BOX. In particular, dynamic back-biasing is an extremely efficient power management technique to either significantly boost performance or cut leakage – especially as, at advanced nodes, FD-SOI enables obtaining much more marked effects on performance than what bulk CMOS can achieve with the similar technique of bulk body biasing (FD-SOI transistors exhibit a VT shift vs applied back-gate voltage of the order of 70 to over 170mV/V, depending on BOX thickness etc. <Andrieu2010>).

In this respect, a notable additional advantage of FD-SOI is that the back-bias voltage can be set to much higher values. On bulk, the limiting factor is the leakage of source and drain junctions to substrate, limiting the forward bias to 200-300mV. On FD-SOI, the limiting factor is the p-n junction between wells. Assuming symmetric biasing of the N-well and P-well, the forward bias can reach VDD/2 and even a little more if some positive biasing of the junction between wells is accepted. Refer to A-3-2 for details.

A frequent question is the following: “Is introduction of (‘active’) back-bias mandatory to port a SoC to FD-SOI ?” — considering that the objective of the port is to bring at same VDD a performance boost for comparable or better overall leakage power (or, therefore, lower VDD hence dynamic power savings for the same performance).

Here we are assuming that there is good correspondence between the VT menu used by the SOC on Bulk and the FD-SOI ‘native’ (that is, without active back-biasing) device menu offered by the foundry (*). In other words, a set of VT flavors with Ioff comparable to those of the original bulk design is available natively in the FD-SOI device menu – although, as mentioned in 3.7, deviations from this situation may be acceptable. Then, remapping the SOC mostly by swapping Bulk devices and cells for their FD-SOI counterparts is possible. Introduction of (active) back-bias is NOT mandatory. The SoC will benefit from the intrinsic advantages of FD-SOI by simple porting.

Then, depending on the efforts that can be afforded, there is the option to do more back-bias specific design and push further the FD-SOI advantage by introducing dynamic back-bias as an efficient power management technique.

Possible Impact: Physical Implementation of SoC building blocks and SoC Top Level Integration

(*) If this is not the case, then the set of native VT may be brought to more suitable values by static back-biasing, as outlined in Appendix A, with more impact on SoC porting.

4. Impact per Design Domain

4.1 Logic Library Cells

Standard Cells:

Direct Porting is a viable option if worthwhile benefits and fastest time-to-market are sought. That involves using the same standard cell design and layout, swapping Bulk devices for FD-SOI devices with same geometry (W/L), and re-characterizing the cell.

Alternatively, re-optimization of selected cells e.g. by tuning transistors W/L vs. exact transistor characteristics may help further improve performance. The exact gain to expect and the return on efforts can only be confirmed by checking the specifications of the FD-SOI technology offered by the foundry.
**Substrate Tie Cells:**

Substrate tie cells used in bulk CMOS technology need to be updated into “buried-well tie” cells for usage in an FD-SOI design: the bias voltages (Vdd/Gnd, or other) need to be applied to wells now located underneath the BOX, as explained below.

In FD-SOI, the very thin active silicon sits on top of the buried oxide and is not embedded in wells. However, wells may now be required under the BOX. They are necessary if back-bias is used (in which case they are typically combined with heavily doped back-planes -- see Appendix A). It is likely that they are also used when no 'active' back-bias is required, just to tie the back-gates to Vdd/Gnd and avoid any “floating back-gate” disturbance. The difference between a bulk substrate tie and an FD-SOI substrate tie is that the contact to substrate in FD-SOI is made through the top silicon and the BOX. From a chip layout point of view, this is transparent. This is illustrated in the notional figures below (Fig. 4 – Well biasing and ties in Bulk Technology – Notional Cross-Section & Top View and Fig. 5 – ‘Buried-well' biasing and ties in FD-SOI – Notional Cross-Section and Top View) – for simplicity no heavily doped back-plane (typically required just below the BOX if back-biasing is implemented) is represented.

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**Antenna Protection Cells:**

In bulk CMOS technology, protection against “antenna-effects” is typically ensured by fulfilling Antenna Rules from the Design Manual, which make sure that at no time during the fabrication process a long metal wire connects to a transistor gate and not yet to the diffusion area of the driving logic gate. These Antenna Rules maybe complemented by Antenna Protections diodes inserted close to the victim gate when the above rule cannot be fulfilled just by playing upon metal routing.
With FD-SOI:

> One difference between bulk CMOS and SOI has to do with the antenna effect mechanism. In bulk CMOS, only the gates of transistors connected to long routing wires are potential victims during chip fabrication. The driver side (i.e. diffusion area of transistors) is at no risk: charges cannot build up on the metal lines connected to a driving logic cell, because they get evacuated into the substrate by the n-p junction of the driving FET before reaching a harmful level. In SOI, however, the diffusion area of the driving logic gate is isolated from the substrate by the BOX and can also be harmed by charge building up on large floating nets during fabrication. One solution that has been used in SOI involves regularly connecting power supply nets to the substrate, through the BOX, thereby providing a discharge path (with transistors behaving as shunt elements during fabrication) [Hook2008].

> The antenna protection diode cell needs to be modified. In Bulk, it typically consists of a diode between M1 and the substrate. In FD-SOI, the presence of the BOX must be taken into account. Updating the FD-SOI antenna diode cell could typically involve opening up the BOX to give access to the underlying bulk substrate and build the diode there – taking into account the possible presence of a well and back-plane under the BOX (which will be biased during operation).

4.2 Memory Compilers

Pre-requisite for easy porting: the bitcells provided in the FD-SOI PDK should be footprint compatible (i.e. same abstract) with those provided in the Bulk CMOS PDK. (It is possible that the bitcell itself, provided in the PDK by the foundry, is not a direct port from the Bulk bitcell – but this is transparent to the designers that use it).

It is assumed here that the foundry provides counterparts to bulk bitcells that have better performance at comparable or better leakage (without having to adjust VTs by static back-bias), and the periphery can also swap bulk devices for their FD-SOI counterpart because VT (or Ioff) are comparable. Then the same compiler can be used, with updated characterization (timing, power, etc.). Bulk substrate ties are to be replaced by FD-SOI substrate ties (contact to substrate through the top silicon and thin buried oxide, to avoid leaving the substrate floating) – but this may be handled globally (for all substrate ties) at mask generation rather than at individual memory compiler level.

For the periphery, options are the same as for standard cells: direct port for fastest time-to-market or re-optimization, e.g. for optimal p/n ratio.

If the original bulk compilers did already include body-bias features – typically as Read-assist/Write-assist/SNM improvements techniques – Bulk body-bias translates fairly directly as Back-Bias in FD-SOI. Bulk substrate ties (to carry bulk body-bias voltage) need to be swapped for FD-SOI substrate ties (to carry FD-SOI back-bias voltage).

Then there is always the option to introduce new and specific optimizations for optimal SRAM figures of merit, as suggested in <Yamaoka2006> for example; however this diverges from the simple design porting approach.

4.3 I/Os and ESD protections

I/O cells use not only FET devices, including thick-oxide transistors, but also non-FET devices. Integration of thick oxide transistors on FD-SOI is not an issue and has been demonstrated [Fenouillet2009, Cheng2009]. Regarding non-FET devices, most of them will have a counterpart in the FDSOI device menu offered by the foundry. Depending on the strategy adopted by the foundry, some of them may actually be provided as Bulk devices, through Bulk-FDSOI co-integration (by locally etching off the top silicon and the BOX to give access to the underlying Bulk substrate).
4.4 Analog and Mixed Signal IP

**Devices:**
Like IOs, analog IPs use not only FET devices, including thick-oxide transistors (demonstrated on FDSOI), but also non-FET devices. Most non-FET devices typically used in an original analog IP design on Bulk will have a counterpart in the FDSOI device menu offered by the foundry. Depending on the strategy adopted by the foundry, some of them may actually be provided as Bulk devices, through Bulk-FDSOI co-integration (by locally etching off the top silicon and the BOX to give access to the underlying Bulk substrate). For example, the following devices have been demonstrated in an FD-SOI flow, without resorting to Bulk co-integration: Resistors (poly, epi), Capacitors (MOSCAP, MIM), Varactors, Lateral
Diodes, BEOL Inductors [Monfray2010, Cheng2010] while devices such as substrate diodes or bipolars may resort to Bulk co-integration.

It might however happen that some devices used in the original Bulk design have no direct counterpart in the FDSOI device menu offered by the foundry, be it natively or through co-integration. Then it is necessary to adapt the analog design to come up with a solution based on the available devices.

Key Figures of Merit for Analog Design and their Rating in FD-SOI:
The following table outlines the key figures of merit for Analog Design (some of them are inter-related).
The excellent electrostatic control of transistors and the absence of intentional channel doping go in the direction of improving these parameters (vs. bulk CMOS technology) and enabling even fairly small analog transistor to behave very well.

Nevertheless, today there is only limited published silicon data allowing to quantify this for ultra-thin BOx FD-SOI technology. One relevant study is [Kilchytska2011]: the trends indicated in the table below mostly rely on this study; they will need to be confirmed.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Trend in FD-SOI / UTBOX vs. Planar Bulk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transconductance to drain current ratio:</td>
<td>Positive trend (*)</td>
</tr>
<tr>
<td>$G_{m}/I_{d}$ vs. $I_{d,norm} = I_{d}/(W/L)$</td>
<td><em>(channel orientation dependent)</em></td>
</tr>
<tr>
<td>$G_{m,max}$ at fixed $I_{d,norm}$</td>
<td></td>
</tr>
<tr>
<td>Early Voltage: $V_{EA}$</td>
<td>Very positive trend (*)</td>
</tr>
<tr>
<td>Intrinsic Gain: $A_0$ or $g_{m}/g_{d}$</td>
<td>Very positive trend (*)</td>
</tr>
<tr>
<td>$G_{m}/I_{d} x V_{EA}$</td>
<td></td>
</tr>
<tr>
<td>Transition Frequency / Gain x Bandwidth $F_T \sim G_{BW}$</td>
<td>Positive trend (*)</td>
</tr>
<tr>
<td>$= G_{m}/2 \cdot I_{d} \cdot C_{L}$</td>
<td></td>
</tr>
<tr>
<td>$1/f$ Noise</td>
<td>Positive trend (**)*</td>
</tr>
<tr>
<td>Thermal Noise</td>
<td>Positive trend (**)*</td>
</tr>
<tr>
<td>Temperature Stability</td>
<td>Positive trend (*)</td>
</tr>
<tr>
<td>VT Matching</td>
<td>Positive trend (***)</td>
</tr>
</tbody>
</table>

(*) Based on [Kilchytska2011], (**) Based on [Flandre2010], (***) Based on [Andrieu2010]

Still, in the context of design porting, improved figures of merit at transistor level do not necessarily directly translate as improved behavior of the circuit vs. the target specification without some design tuning.

Analog and Mixed Signal IP Porting Efforts:
Broadly speaking, the approach required is expected to be:
- start from the micro-architecture of the original Bulk design
- resize devices and tune bias points, targeting devices from FD-SOI library,
- tune or re-do layout, extract parasitics, iterate until design specifications are met

The amount of changes actually required will depend on the type of Analog & Mixed Signal IP. One factor that may, in certain cases, alleviate the work required is the expected lower sensitivity of FD-SOI to PVT corners – for example, keeping the same W/L for a transistor could lead to a different current in nominal conditions and still deliver current values that are within specs in corner cases.

When design tuning effort is required, it is also an opportunity to leverage the superior characteristics of FD-SOI analog transistors, and thereby obtain much better behaved analog IPs.
Below are some additional indications, per category of Analog IP typically found in an SoC built in advanced CMOS technology. Not all of these IPs are necessarily required in the target SoC, however at least some PLLs/Frequency Synthesizers/DLLs are normally present for clock generation, as well as some sort of high speed PHY (at least external memory interface).

**PLL, Frequency Synthesizers, DLLs:**
Factors to take into account include: faster propagation times through delay elements, lower parasitic capacitance. Resizing of devices must be considered – otherwise, for example: keeping the same target frequency could require either to lower the power supply (if voltage controlled) hence risk of degraded SNR, or to lower the current (if current controlled) hence risk of increased phase noise and jitter. Note that varactors on FD-SOI are expected to offer a good tunability range (because of reduced parasitic capacitance).

**High Speed PHYs:**
These are the physical interfaces of high speed links to the external world – typically DDR memory interfaces, also possibly MIPI, USB, HDMI, etc. Some sort of Serializer/Deserializer is an often-found building element. Although these PHYs carry digital data, they are often treated as Analog and Mixed-Signal blocks because their design is critical and they have very tight specs on data phasing, eye-diagram opening etc.
Aspects that could help here are:
- reduced variability,
- faster charging/discharging of output node, improving data-dependent jitter and therefore eye opening [Kamel2009].

In a SerDes, the output stage is a critical analog block, whose current is typically imposed by load and voltage swing specifications. Therefore, in the context of design porting, the output stage needs to be resized to maintain this target current.

**D/A Converters, Amplifiers:**
There is a clear opportunity to design excellent amplifiers and D/A converters on FD-SOI, exploiting in particular the improved intrinsic gain and gain x bandwidth products expected from FD-SOI analog transistors. This however comes with design tuning effort rather than direct porting.

**A/D Converters:**
The design of A/D Converters often depends on multiple inter-related parameters and second-order parameters. As a result, some more significant design tuning work can probably be expected, although there has been limited published work about A/D converters on FD-SOI.

**Self-heating:**
For Analog IP that involve relatively large amounts of DC or quasi-DC current (i.e. maintained for periods at least commensurate with the self-heating time-constant – which is device architecture dependent, for example [Polonsky2004] reports of the order of 100ns for thick BOX, should be more on thin BOX), self-heating may come into play and may need to be taken into account in SPICE simulations if very accurate control of currents is required to meet the specifications.

### 4.5 SOC Porting

#### 4.5.1. Path1 - ‘Straight SoC Porting’

We are considering here the case where the least possible effort is required (that is, where the ideal case would be reusing the GDS as is) – i.e. no efforts on FD-SOI specific design that could bring further advantages.
That implies there is no willingness to introduce any “active” back-biasing scheme (as defined in section 3.8) into a design that did not use body bias in the original bulk version. If, however, the original bulk design did already use body bias then this can be simply transposed as back-bias in FD-SOI.
**SOC Physical Implementation Aspects**

Physical implementation covers aspects such as floorplanning, cell placement, routing, etc. If direct SOC porting is sought, it is reasonable to assume that the building blocks used in the SOC (standard cells, memories, I/Os etc) have been ported (possibly just re-characterized) at constant footprint – in other words the physical views of these building blocks are either identical or have same abstract as in the bulk version.

Then, also considering that the foundry has made technology implementation choices such that there is no need to introduce (active) back-biasing to properly set the target VTs, only limited changes are required in the SOC physical implementation. The same placed and routed digital blocks and top-level SoC integration can be used, with bulk library cells, memories, I/Os and AMS blocks swapped for their FD-SOI counterpart. Among library cells, the physical structure of a few cells – mostly substrate tie cells and possibly antenna protection cells – definitely need to be updated, which can actually be handled through automatic swap when generating the mask GDS.

**SOC Sign-Off Aspects**

Signing off a SOC design that has been ported from Bulk to FD-SOI will involve re-running a number of checks like Timing Checks, Design Rules Checks (incl. Antenna Rules), etc. on the design database. The design database needs to be updated to point to IPs and to library views updated for the FD-SOI technology (for example, re-characterized standard cells). Violations, if any, will have to be fixed by ECO (Engineering Change Order), as is classically done at the final steps of sign-off of a bulk design.

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*Fig. 7 – Path 1: Porting a SOC (digital part) from bulk CMOS to FD-SOI at minimum effort*
4.5.2. Path2 - With insertion of back-bias

We are now considering that the design team is prepared to invest in a little more specific design to enjoy further benefits of the FD-SOI technology. Specifically we will consider the case where designers want to exploit the potentiality of back-bias for additional performance boost or leakage reduction.

Physical Implementation Aspects

Power nets carrying the independent voltages required for back-biasing must be inserted, and routed in such a way that sufficient integrity of these voltages is achieved. In addition, adequate voltage sources are needed and different options exist:

1) Back-biasing voltage supply may be external to the chip, in which case dedicated power supply I/Os must be included in the chip.
2) Or, the voltage sources may be generated on-chip, in which case the suitable IP block must be included in the chip.
3) A third option is to design the back-biasing scheme to live with already voltage sources already available on-chip (for example, 1.8V already used for IOs or Analog).

Sign-Off Aspects

The design database now also needs to reflect any of the physical changes outlined in the former paragraph. The sign-off flow, identical to that used in bulk, must be run on this updated design.

Note that one of the key challenges to sign-off designs in recent Bulk technology should be alleviated with FD-SOI: With recent Bulk technology, variability and process variations have become so large that there are paths that can hardly be fixed for both hold and set-up times whatever the operating condition corner; Now because FD-SOI is normally less subject to variability and process variations, timing sign-off should be easier. Combined with lower dependency of performance to power supply voltage, this may be particularly interesting in the context of Multi-Mode Multi-Corner simulations.
4.5.3. Alternative Case

In the case where the foundry did not align its native VT offering in FD-SOI with its bulk offering, then the design could rely on static back-bias to set the target VTs. In that case, Path 1 described above does not apply and we are back to the Path 2 – the physical implementation has to be updated to cope with static back-bias insertion (unless the original bulk design already implemented body bias).

5. Design Techniques

The design techniques classically used in Bulk CMOS are compatible with FD-SOI. One particular case is body-bias (i.e. shifting well bias voltage away from Gnd/Vdd), which must be transposed as back-bias on FD-SOI: the principle is essentially the same, with bias voltage now applied under the BOX of the target transistors.

In the context of a direct porting of a full SOC from Bulk to FD, the extent to which the system will actually benefit from the performance/power advantage of FD-SOI depends on the flexibility of the power management techniques implemented in the original design that gets ported.

For example – Assume a block that reaches a specified frequency in Bulk: its power supply could be lowered by e.g. 100-200mV in FD-SOI for the same target frequency. Assume another block that needs to run as fast as possible, with FD-SOI it can run significantly faster than in Bulk with the same power supply. If both blocks are in different voltage islands and rely on different power supplies, then both
benefits can be enjoyed. If, however, these blocks rely on the same power supply, then it’s either one benefit (faster frequency where needed, at same global Vdd – therefore no substantial power saving) or the other (lower dynamic power owing to globally reduced Vdd, but no frequency boost).
APPENDIX A : BACK-BIAS

A-1. Objectives of Back-Biasing

In the different published works on FD-SOI, back-biasing is essentially envisaged for two distinct purposes:

1/ as a Power Management Design Technique, either to temporarily (i.e. dynamically) boost performance (forward back-bias) at the expense of leakage during that time, or to cut leakage (reverse back-bias) at the expense of performance (typically, during idle periods).

Or:

2/ as a means to statically shift a set of VTs to values different from the native VTs:
   - in the technology offered by the foundry, a set of distinct, "native" VTs is obtained by different gate stacks and/or any other selected method (as outlined in Appendix B).
   - and block-wide static back-bias enables to shift this "native" set of VT to a different set of VT, thereby enabling, for example, to serve the needs of multiple types of SOC from a relatively reduced set of VT.

In the application, from chip to chip, the biasing voltages used may either always be the same (fixed back-bias) or be adaptively tuned on a per-chip basis e.g. for process compensation (adaptive back-biasing). However, defining target VTs for the application through static global back-biasing is less "porting-friendly" than relying on suitable native VTs, as more design re-work is needed for SOCs that did not use body biasing on bulk.

Note – It is not expected back-biasing would be used to define freely mixable, multiple VTs from a single type of transistor, as this would require applying independent back-bias at transistor or standard cell level, which would be overly complex.

A-2. Back-Biasing Principles

Back-biasing consists of applying a voltage under the thin BOx, thereby changing the electrostatics of the transistor and shifting its Ion/Ioff operating point (or, equivalently, shifting its threshold voltage VT). The general behavior is illustrated by the notional curve below. The back-bias voltage applied may be constant or may switch between different values, depending on intended usage.
In practice, back-biasing is normally associated with the presence of a heavily-doped “ground-plane” or “back-plane” just below the BOX, implementation in the technology is outlined further down this appendix. It has been determined that under some conditions, response to back-biasing is better for transistors with a back-plane [Fenouillet2010]. This back-plane is also useful for Multi-VT implementation, as described in Appendix B, and for better electrostatics [Andrieu2010]. Fig. a.4 outlines the effects of combined back-biasing and back-plane (refer to [Noel2011] for more quantitative experimental results). In practice the exact behavior depends on BOX thickness and is slightly different for a p+ and for an n+ back-plane.
A-3. Implementation of Back-Biasing

A-3-1. Back-biased Transistor Structures

In a chip, implementing back-bias requires bringing a bias voltage underneath the BOx of transistors, as outlined in Figure a.5. A contact is made between a biasing voltage source and the substrate, through the top silicon and the BOx. Electrical continuity under the BOx is ensured by an N-type or P-type well implanted under the BOx. In this example, PFETs and NFETs are biased independently.
The required density of substrate ties will be defined by Design Rules of the technology. It is expected to be lower than the density required for Bulk substrate ties, as the primary factor that defines this density in Bulk is latch-up prevention – which is not a concern in FD-SOI owing to the presence of the buried oxide and resulting full device isolation.

![Image](https://www.soiconsortium.org)

**Fig. a.6: Back-Biasing through well continuity (outline view)**

A-3.2. **FD-SOI Back-bias vs. Bulk CMOS Body Bias**

Back-biasing is similar to body biasing used in some bulk designs. However, the biasing voltage is applied under the BOx and electrostatic coupling is through the BOx. FD-SOI Back-Biasing exhibits a number of advantages over Bulk Body-Bias, in particular:

- While Bulk (forward) body bias is typically limited to 200-300mV (otherwise the Source and Drain p-n junctions to substrate start to turn ‘on’ and too much leakage current starts to flow), there is no such problem in FD-SOI because source and drain are fully isolated from the substrate by the buried oxide. As a result it is possible to bias the N-well and P-well to much higher voltages. In a classical transistor and well architecture such as that depicted above, the limiting factor is the P-N junction between wells, limiting the forward bias to VDD/2 (assuming symmetric bias of the wells), or a little more if some positive biasing of the junction between wells is accepted.

- While the effectiveness of Body Bias tends to sharply degrade as transistor dimensions shrink and become relatively ineffective at the 20nm node, this is not the case for back-bias in FD-SOI which retains excellent dVT/dV values in small geometries, provided the BOx is thin enough (see for example [Andrieu2010, Noel2011]).

A-3.3. **Practical Implementation in Circuits – Block-level Back-biasing**

Multiple implementations and usages of back-bias can be envisaged. The most likely implementation, keeping complexity reasonably low, is at block-level or possibly die level (Fig. a.7). If there are different back-biased “islands” (like Block1, Block2, Block3 in the figure) and these use independent Pwell biasing voltages (Vback-nfet), a triple well or deep N-well implementation should be used.
In order to apply the proper bias voltage, special cells that contact the substrate (P-well and N-well) to the intended voltage sources (V\textsubscript{back-nfet}, V\textsubscript{back-pfet}) must be regularly inserted in the design. The maximum distance between these contact cells will be defined by the Design Rules of the Technology. This is extremely similar to the substrate ties required in Bulk CMOS designs to bias the N-Well and P-Well Bulk substrate.

For standard cells, this is illustrated in the following figure.
And for SRAM memory arrays:

![Fig. a.9: Back-Bias implementation in SRAM arrays (notional)](image)

The same concept applies to other physical blocks, including Analog IPs or I/Os. If their transistors need to be back-biased, contacts will be inserted with a minimum density defined by the Design Rule Manual and will create an electrical connection between the relevant biasing power supply net and the relevant well placed under the BOX.

### A-4. Usages

#### A.4.1. Usage 1: Dynamic Performance Boost / Leakage Cut-Off

It may be interesting to temporarily trade-off leakage and power consumption of some blocks for peak performance. For example, when downloading a web page, it may make sense to temporarily push the performance of the CPU subsystem. This can be achieved by applying Forward Back-Bias. Operating frequency improvements up to 20% have been reported with this technique [Fenouillet2010, Skotnicki2010].

Conversely, in some other scenarios it may be interesting to keep minimum functionality and cut leakage as much as possible. This may for example be the case of SRAMs in stand-by mode with data retention, or logic blocks in sleep mode. This can be achieved by applying Reverse Back-Bias. Impressive off-current improvements have been reported with this technique [Andrieu2010].

This is “semi-dynamic” back bias in the sense that the bias value will be modified over time, but it is acknowledged that the capacitive loading of the wells is such that the transition from one biasing state to the next will take time. This transition could typically take several micro-seconds. This is not an issue as long as it is understood that this mode of operation requires switching from one operating scenario to another one at application level, and the chip typically remains in the selected biasing state for several seconds or more. The timescales involved with dynamic back-bias may for example be similar to those involved in the widely used Dynamic Voltage and Frequency Scaling technique (DVFS, whereby power supply and operating frequencies of full blocks are adjusted under application control according to the ongoing usage).
A.4.2. **Usage 2: Static VT Shift (block-level)**

Assume a technology that includes a number of “native” VT flavors. The native VTs are those obtained without ‘active’ back-bias (typically, with Nwell under the BOx simply tied to Vdd and Pwell tied to Gnd – similar to Bulk). The way these native VT are obtained (gate stack work-function, doped back-plane…) is not relevant here.

From this set of native VTs, it is possible to define a different set of target VT usable by the application by applying back-bias. This would be done at block level, meaning all transistors in this block see their |VT| shifted in the same direction by a comparable delta (in practice the shift may not be exactly identical for all VTs and may slightly differ between NFET and PFET).
**A.4.3. Option: Adaptive VT tuning**

When one of the above mechanisms is in place, it can be complemented by an adaptive mechanism whereby the exact back-bias voltage applied can be tuned to compensate for inter-die variations. By detecting whether the die is in a “fast-and-leaky” process corner (corresponding to VTs lower than nominal) or in a “slow-and-low-leakage” corner (corresponding to VTs higher than nominal), either at electrical wafer testing stage or in the application, it is envisageable to compensate for that and have even more stable VT from die to die.

**A.4.4 More complex schemes**

Other schemes are possible, according to designers’ needs and imagination. Examples include mechanisms to increase SRAM noise margin or writability as reported by e.g. [Yamaoka2006].

**A-5. Area Impacts**

- **Substrate Ties**:
  FD-SOI on ultra-thin BOX exhibits good receptivity to back-bias, that is fairly large dVT/dV_{bs} [Andrieu2010]. This could also mean that any voltage drop of the bias voltage between a transistor and the nearest back-bias contact causes more unwanted VT shift in the case of FD than in that of Bulk. Therefore that could require more (i.e. less spaced away) back-bias contacts in the case of FD. However, the driving factor for substrate ties density in the case of Bulk is more latch-up prevention than bias voltage drop. As latch-up is not a concern for FD-SOI, it is expected that the number of well ties effectively required in the case of FD-SOI is actually less than that required in the case of bulk CMOS.
  So, having back-bias in FD-SOI should not entail an area penalty due to back-bias contacts, and simply swapping bulk CMOS well ties for FD-SOI buried-well ties should be a conservative approach. Of course, this will only be confirmed by Design Rules provided by the Foundry.

- **Dedicated Back-bias voltage power rails (if needed)**:
  If active back-bias needs to be introduced into a design, it is necessary to route dedicated power nets from bias voltage sources to the well ties, paying attention to noise. That is going to consume some
routing resources. The impact should depend on the utilization ratio of routing resources, but is not expected to be very significant – for example, [Narendra2002] reports an area increase of the order of 1% for back-bias power net routing.

- **Back-bias voltage sources (if needed):**
  * Case 1 - If dedicated embedded voltage sources are used to generate the specific back-bias voltages: these voltage generators will eat up some area.
  * Case 2 - If the back-bias voltage sources are external and connect to the chip via some specific IOs: then there may be an impact due to insertion of new IOs.
  * Case 3 - No area impact due to biasing voltage sources if existing on-chip power supplies are shared to bias the substrate.

Overall: if 'active' back-bias is required, its introduction would have a small, although not null, impact on die size (vs. the area consumed for regular well biasing in a planar Bulk reference), due to the need for a power grid to carry bias voltages plus possibly the introduction of back-bias voltage sources. If, conversely, no active back-bias is required and any wells present under the BOx only require standard biasing to Vdd and Gnd (see Fig. 1.b) then no area impact vs. a planar Bulk reference is expected.
APPENDIX B: ‘NATIVE’ MULTI-VT in FD-SOI

While Multi-VT in Planar Bulk CMOS technology is achieved by multiple channel implants, this approach is normally not used in FD-SOI which is essentially an undoped channel technology – enabling the achievement of record-low variability.

Alternative methods to implement Multi-VT in FD-SOI have been investigated and are summed up here. Refer to e.g. [Faynot2010, Noel2011] for details.

We are considering here methods that enable to obtain multiple VT values without having to apply any specific back-bias. The multiple VTs obtained by the methods outlined below are called “native” VTs elsewhere in this document. If the VTs targeted by the applications do not match this set of native VTs, then there is still the possibility to apply block-level back-biasing and thereby globally shift the set of native VT; refer to Appendix A.

Multi-VT transistor solutions are illustrated in Fig. b.1:
- a single (typically mid-gap) metal gate work-function would yield a single VT,
- implementing two metal work-functions (typically, using the same metals in the gate stack as in Bulk HKMG technologies) enables to obtain two VTs,
- implanting a heavily doped back-plane just under the BOX, either n-type or p-type, enables to shift the |VT| by 50-100mV (depending on selected Buried Oxide thickness).
- Combining different back-plane types and dual metal gates enables up to 4 VTs.
- If the VTs achieved with the former approaches still don’t fulfill all the targeted values, some additional knobs are still available, although some of them may involve trading off some figures of merit. Reported possibilities include some level of counter-doping, channel length engineering or alternative materials [Faynot2010].

Fig. b.1: “Native” multi-VT Transistor Solutions
REFERENCES


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DOCUMENT HISTORY

22-Sept-2011: Minor updates following feedbacks.